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Office of Naval Research

Final Technical Report on

Ideal Channel Field Effect Transistors

(N00014-07-1-1134)

July 24, 2007 to March 31, 2009

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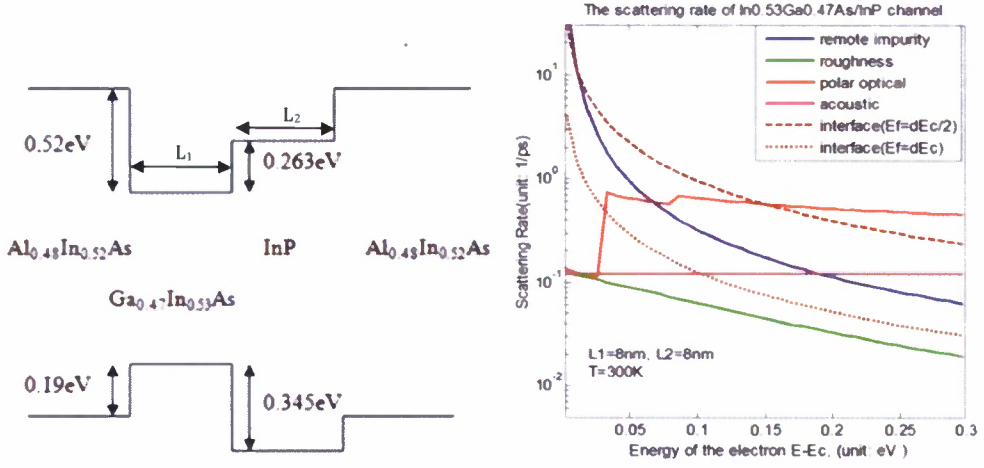
Project overview: Narrow bandgap semiconductors offer high carrier mobilities and low contact resistances while wide bandgap semiconductors offer high breakdown voltages. A series of heterojunction transistors have been investigated and proved to be effective for improving both speed and power output in the past two decades. These devices include double heterostructure InP/InGaAs/InP bipolar transistors and composite channel InAlAs/InGaAs/InP/InAlAs high electron mobility transistors (HEMTs), which have taken the full advantage of the matched lattice constant (or pseudomorphic growth). However, for the most popular wide bandgap semiconductor GaN and SiC, the lattice mismatch between GaN and semiconductors with a reasonably small bandgap (including InGaN) is so large that pseudomorphic growth is very difficult. For instance, the critical thickness of InN on GaN is about one monolayer. To marry the advantages offered by both narrow bandgap and wide bandgap semiconductors, we explored direct wafer bonding for ideal channels made of extremely mismatched materials for field effect transistors. Toward this target, we have performed the following studies. This investigation demonstrated it is feasible to fabricate composite channel transistors, however, more experiments are necessary to understand the effects of the interface between the mismatch materials.

A. Theoretically calculate scattering rates in composite channels.
B. Theoretically calculate breakdown voltage in heterostructures containing wide bandgap material.
C. Experimentally form mismatched GaAs/GaN heterostructures through direct wafer bonding and study the breakdown improvement compared with GaAs/GaAs homojunctions.
D. Experimentally form InGaAs channel on mismatched GaN substrate and fabricate MISFETs on InGaAs/GaN

A) Calculation of scattering rates in composite channels



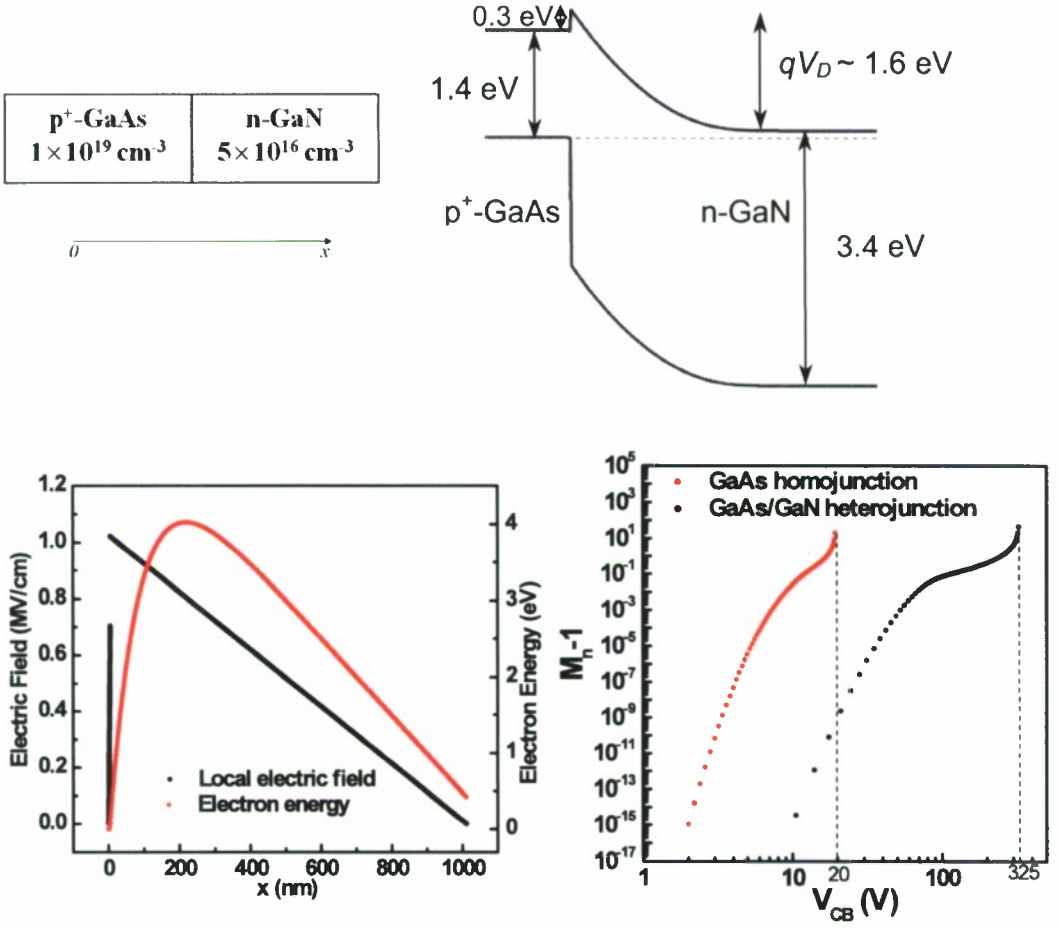
Composite channel FETs can operate at high speed with high breakdown voltages by combining a high-mobility narrow bandgap material and a high-breakdown wide bandgap material. But the heterogeneous integration of dissimilar materials can sometimes induce interface states/charges, thus decreasing the average electron mobility. Therefore, it is important to understand the electron transport property in the presence of the interface states that are often charged in addition to the other scattering mechanisms such as optical phonon, acoustic phonon, and remote impurity (modulation doping). We have calculated various scattering rates of $In_{0.47}Ga_{0.53}As$/InP

composite channels sandwiched by $Al_{0.48}In_{0.52}As$ barrier layers. The scattering rate due to interface charges was calculated by assuming a uniform distribution of donor-type interface states from E_C(InGaAs) to $E_C + dE_C$ where $dE_C = 0.263\ eV$ as shown in the above device structure and a total sheet density of 10^{12} cm^{-2}. The calculated scattering rates are shown in the figure as a function of the electron energy. At low electron energies columbic scattering dominates, therefore, the interface charge scattering rate can be high assuming the electron Fermi level is at the electron energy thus majority of the interface states are positively charged. At high electron energies the polar optical phonon scattering becomes dominant while the columbic scattering rates deceases. These calculations indicate that it is possible the electron transport properties do not suffer severely from the interface states. In the access region, the Fermi level is high above the conduction band edge thus electrons are likely retain a high mobility in spite of the defected but charge neutral interface; in the gated region, electron energies are high thus suffer little from columbic scattering events. On the other hand, these interface states, if present, are expected to trap electrons thus reducing the total number of electrons in the channel; furthermore, conduction due to electrons hopping through these trap energy states is expected to add a slow component in the device current modulation by the gate.

B) Calculation of breakdown voltage of GaAs/GaN

To investigate the advantage of adding wide bandgap materials in improving the device breakdown behaviour, the breakdown voltage of GaAs/GaN *pN* heterojunctions at reverse bias has been calculated and compared with that of GaAs/GaAs *pn* homojunctions considering the avalanche breakdown mechanism. To take advantage of the large critical field of the wide bandgap GaN material, it is important to have negligible depletion region in GaAs. The device structure studied in the calculation is shown in the following together with the energy band diagram. The *p*-type GaAs is much more heavily doped than the *n*-type GaN. Although GaAs has much larger impact ionization coefficients than GaN, electrons do not travel a sufficient distance in GaAs to gain enough energy to induce impact ionization and the breakdown is totally dependent on GaN. The low impact ionization coefficients in GaN can improve the base-collector junction breakdown voltage substantially. The accuracy of breakdown voltage calculation largely depends on the accuracy of electron multiplication evaluation that requires knowledge of the electric field profile. When an electron is injected from *p*-GaAs into the depletion region with high electric fields in *n*-GaN, a finite energy relaxation time is needed to bring the electron energy in equilibrium with the local electric field, i.e. the electron energy lags the local electric field. This non-equilibrium effect makes the impact ionization depend mostly on the carrier energy instead of the local electric field. The electron kinetic energy ($E - E_C$) profile across the junction depletion at a 50 V reverse bias is calculated using the energy balance equation and plotted below, clearly showing that the peak of the electron energy does not happen at the peak local electric field. Therefore the breakdown voltage was calculated using a non-local energy model [Publication 1]. The calculated electron multiplication of p^+-GaAs/*n*-GaAs homojunctions and p^+-GaAs/*n*-GaN heterojunctions is shown below. By replacing the GaAs collector with GaN, the breakdown voltage increases significantly from 20 V to 325 V. Though the calculation was performed in a *p-n* junction thus the modelling could be reduced to a 1-dimensional problem thus being performed analytically, the similar argument can be made to a composite channel FET. In the access region, the electrons largely reside in the narrow bandgap material due to their low energies; and in the gated region toward the drain, the electrons largely reside in the wide bandgap material due to their high energies. Since avalanche breakdown

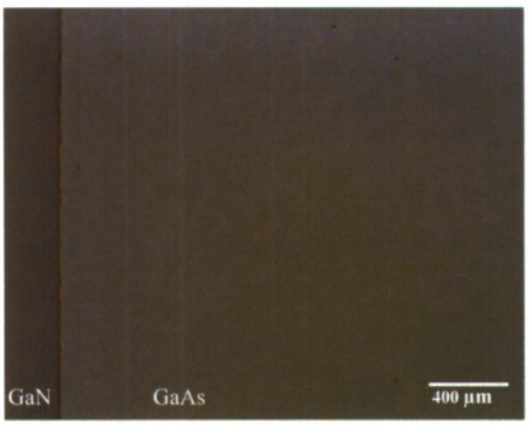
depends on the number of carriers gaining enough energy that can induce an avalanche process while transporting from the source to the drain, and the net number of electrons carrying high energies is very small inside InGaAs in this case, an improved breakdown voltage is expected theoretically. The effects of the interface states can be evaluated experimentally.

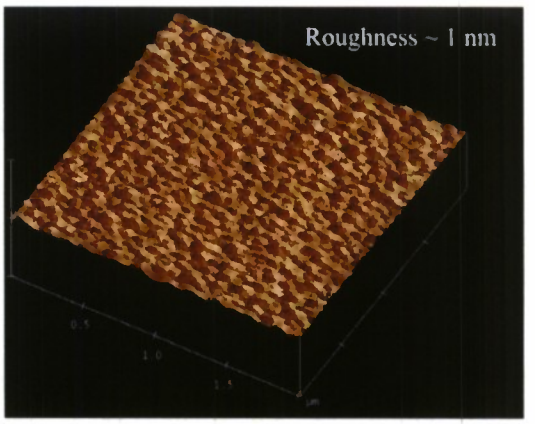


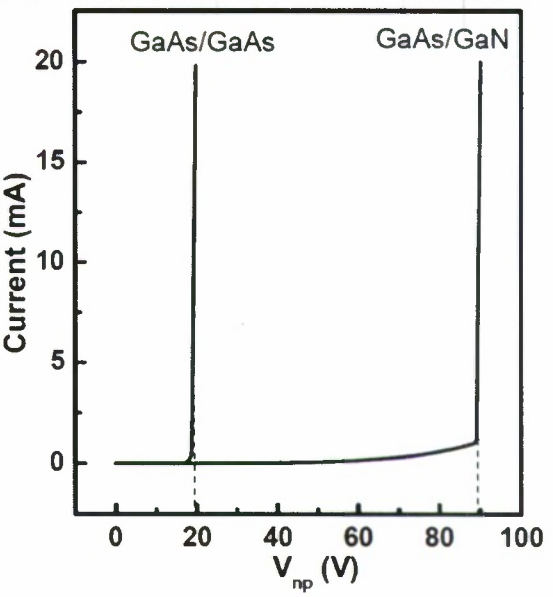
C) Experimental formation of lattice-mismatched GaAs/GaN heterostructure

To start with, GaAs was chosen over InGaAs or InSb because it is binary and easy to obtain. The stable phase for GaAs is zinc-blende. Its lattice constant is 5.65 Å, corresponding to a wurtzite basal plane lattice constant of 4.00 Å. GaN is stable in the wurtzite phase, with a basal plane lattice constant of 3.19 Å. The lattice mismatch of ~ 25% can result in a large number of dislocations in GaAs films epitaxially grown on wurtzite GaN. In this work, we have successfully integrated GaAs with GaN using wafer fusion, also called direct wafer bonding. The wafer fusion process is as follows. After surface cleaning and native oxide removal, the two wafers were brought into intimate face-to-face contact. With an externally applied pressure (~ 5 MPa), the two wafers were bonded at high temperature (550 °C) for 1 h. The GaAs substrate was then removed by mechanical polishing and wet etch. Finally a continuous and smooth GaAs film (100 nm thick) was obtained on GaN, as shown in the optical microscope image and the

atomic force microscope (AFM) image. The advantage of wafer fusion is that the crystallinity of both GaAs and GaN can be maintained except the bonded interface. The transmission electron microscope (TEM) image clearly shows the crystalline lattice structures of GaAs and GaN without dislocations while there is a very thin amorphous material layer (normally 2-5 nm) present at the bonded interface. Diodes were fabricated on wafer-fused *p*-GaAs/*N*-GaN heterostructures as well as on *p*-GaAs/*n*-GaAs homojunctions grown by molecular beam epitaxy (MBE). The diode I-Vs at reverse bias are plotted below. The measured breakdown voltage (~ 20 V) of GaAs homojunctions is in very good agreement with the calculation shown above. Brcakdown improvement (from 20 V to 90 V) is clearly seen when the *n*-GaAs is replaced by *n*-GaN. But the measured breakdown (90 V) of GaAs/GaN is smaller than the theorctical prcdiction (325 V), most likely due to the fact that the calculation presented in section B does not taken account of thc bonded interface that can lead to defected assisted leakage. Nevertheless, the wafer fusion experiments not only successfully demonstrated dislocation-free integration of extremely lattice-mismatched GaAs and GaN, but also showed the improvement in breakdown voltage by employing the wide bandgap material.

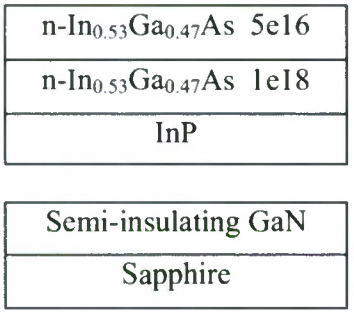


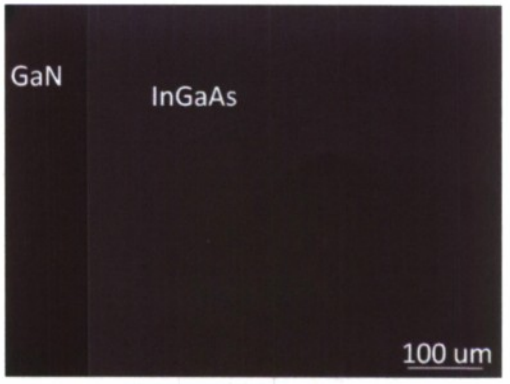


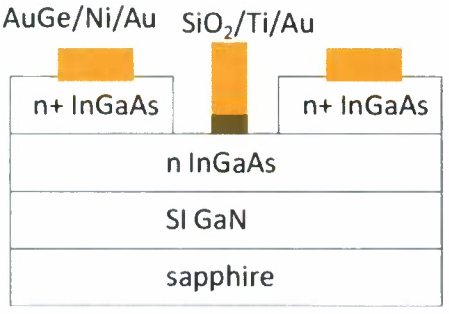


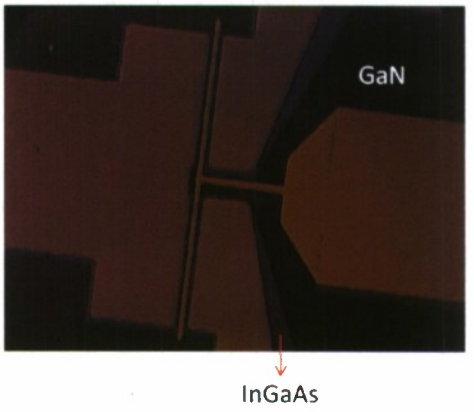
D) Experimental formation of lattice-mismatched InGaAs/GaN heterostructure

After successfully wafer bonding GaAs with GaN, we explored bonding of AlInAs, AlGaAs and InGaAs with GaN. Interesting enough, all of our experiments involving bonding an Al-containing material to GaN failed: the two wafers did not bond together at all after the thermal annealing step. On the other hand, InGaAs bonds with GaN very well at temperatures lower than what is used for GaAs/GaN. An InGaAs/GaN MISFET structure was fabricated and the device layer structures are sketched below. The developed wafer fusion process is similar to that described in section C. After the two samples were bonded together, the InP substrate was removed by mechanical polishing and wet etch in $HCl:H_2O$ (5:1) which stopped at the InGaAs layer. Smooth and continuous InGaAs films were obtained on GaN, as evidenced in the optical images. MISFETs were fabricated on using SiO_2/Ti/Au as the gate stack and AuGe/Ni/Au as the source/drain ohmic contacts.

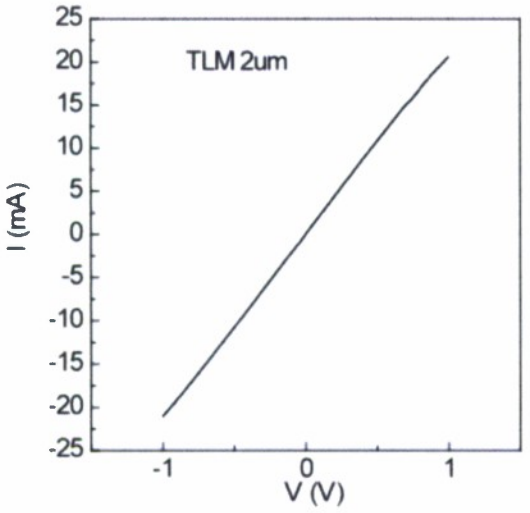


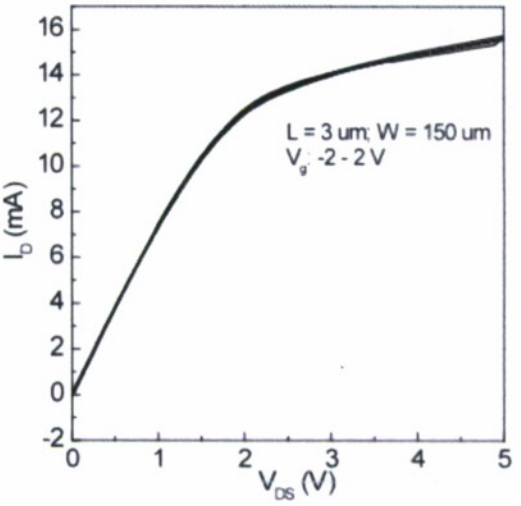






The linear TLM I-V indicated that good ohmic contacts were formed. The family I-Vs show that the drain currents tend to saturate as the drain voltage increases. But there is almost no gate modulation, which is believed due to a large number of interface states at the interface between the e-beam evaporated SiO_2 and InGaAs. Unfortunately the atomic layer deposition (ALD) was not available to us during this investigation. A series of studies have been published in the past few years demonstrating inversion-type InGaAs MOSFETs employing ALD high K dielectrics. Therefore, we expect that using an ALD high K dielectric, it should be possible to fabricate wafer-fused InGaAs MISFETs.





Personnel supported: 2 graduate students

Equipment purchased: none

Publications/Presentations:

[1] Chuanxin Lian and Huili Grace Xing, "The role of setback layers on the breakdown characteristics of AlGaAs/GaAs/GaN HBTs", *Phys. Status Solidi (c)* 5, 1989 (2008)

[2] Chuanxin Lian and Huili Grace Xing, *51st Electronic Materials Conference*, University Park, PA, USA (June 2009): The dominant gain limiting mechanism in wafer-fused AlGaAs/GaAs/GaN HBTs

[3] Zongyang Hu, Chuanxin Lian, and Huili Grace Xing, *52nd Electronic Materials Conference*, Notre Dame, IN, USA (June 2010): AlGaAs/GaAs/GaN wafer fused HBTs with Argon implanted extrinsic collectors

[4] Chuanxin Lian, Huili Grace Xing, Yu-Chia Chang, and Zhen Chen, "Temperature dependent study of AlGaAs/GaAs/GaN HBTs", in preparation

[5] Huili (Grace) Xing, Zongyang Hu, Chuanxin Lian, "Transistors formed by wafer fusion", University Government Industry Micro/nano symposium (UGIM), West Lafayette, 2010.